

**A 700/900mW/Channel CMOS Dual Analog
Front-End IC for VDSL with Integrated
11.5/14.5dBm Line Drivers**

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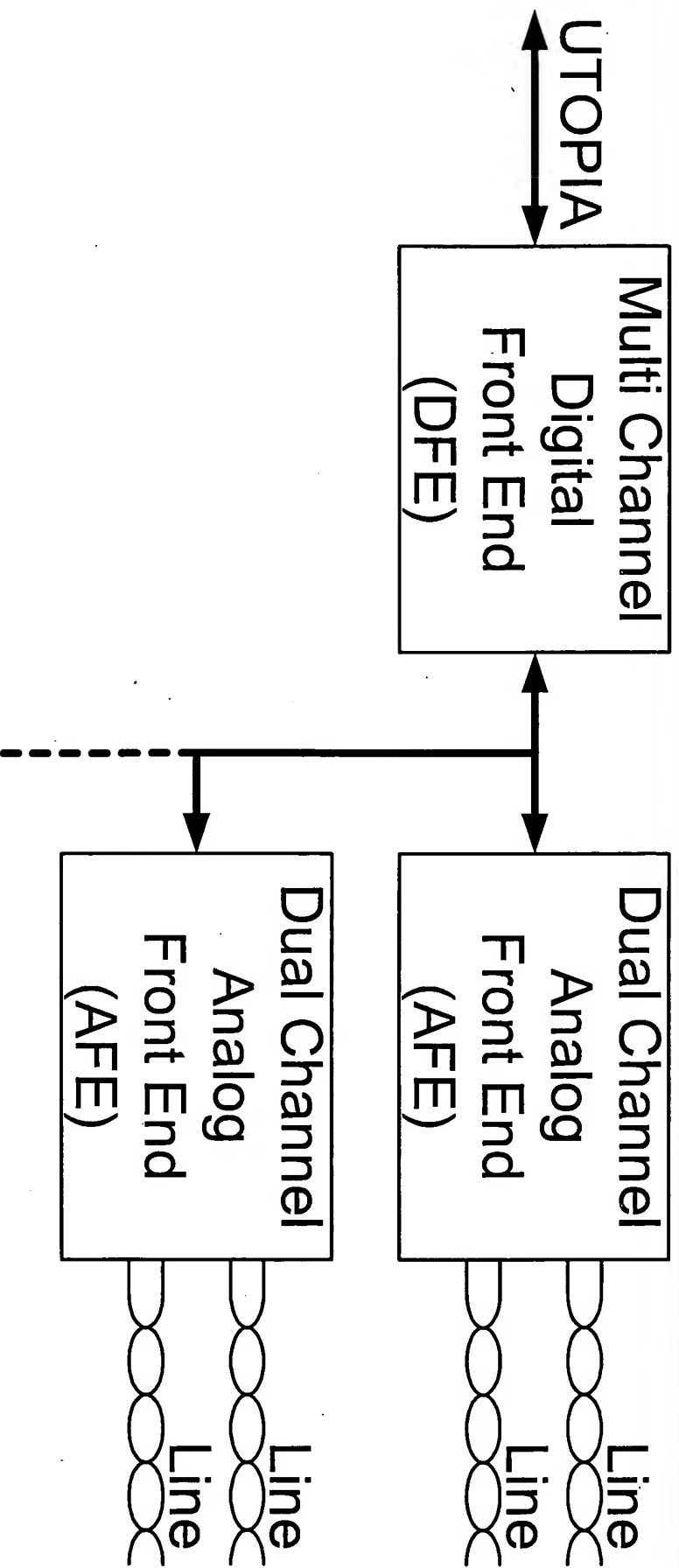
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Outline

Dual Channel VDSL AFE

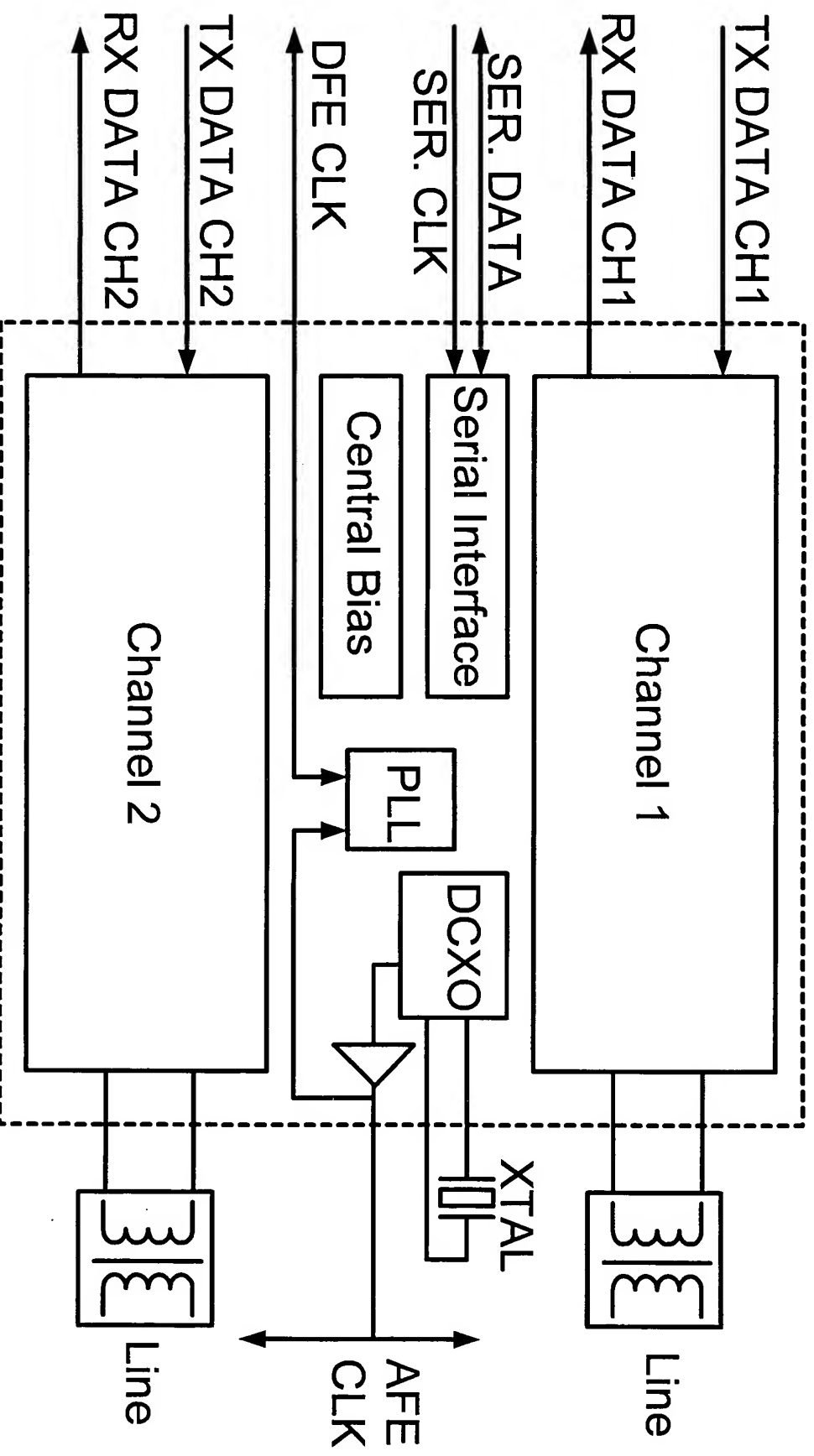
- Overview
- Architecture
- Circuit Implementations
- Measured Performances
- Summary

Overview

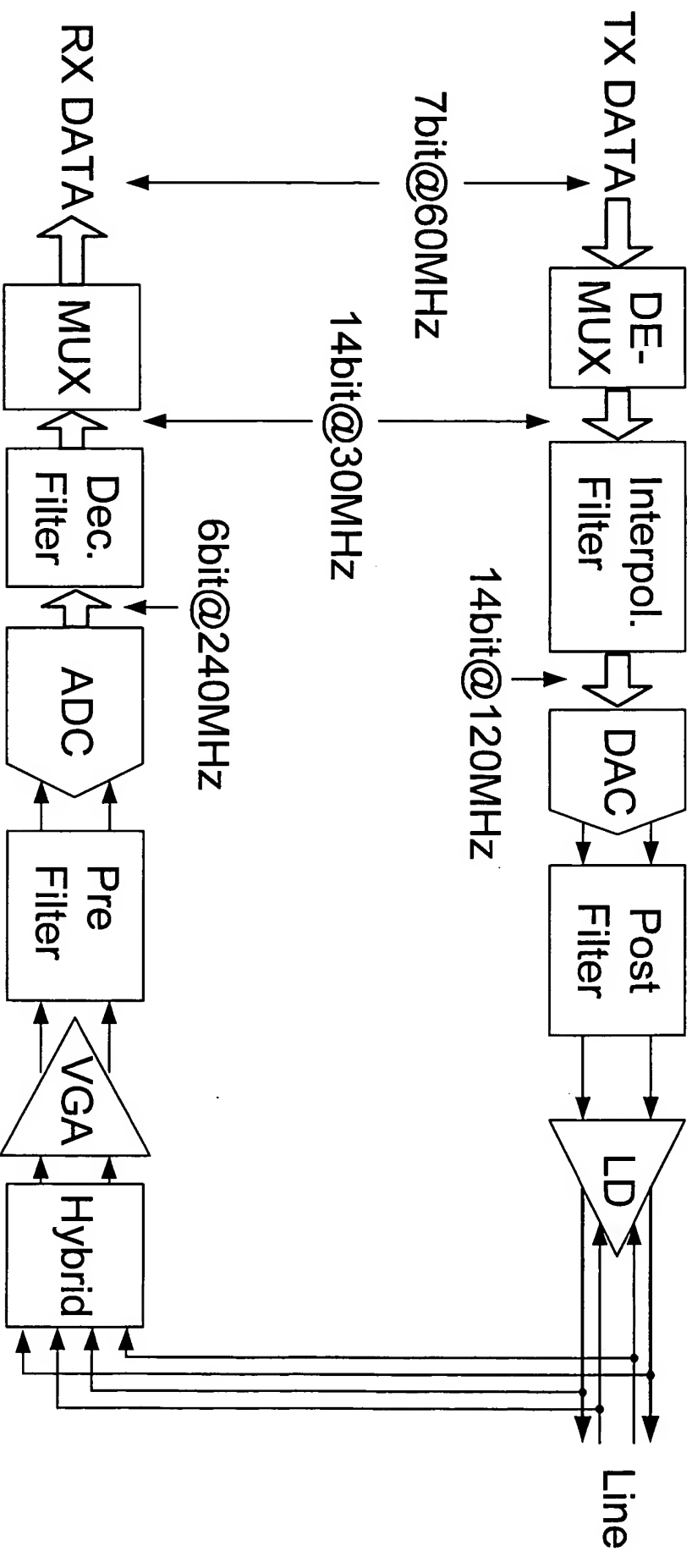


- VDSL-AFE for CO and CPE
- 0.25/0.5 μ m 5M 1P CMOS, MIM-Capacitors, Poly-Resistors
- Emphasis on power saving
- Almost no external components

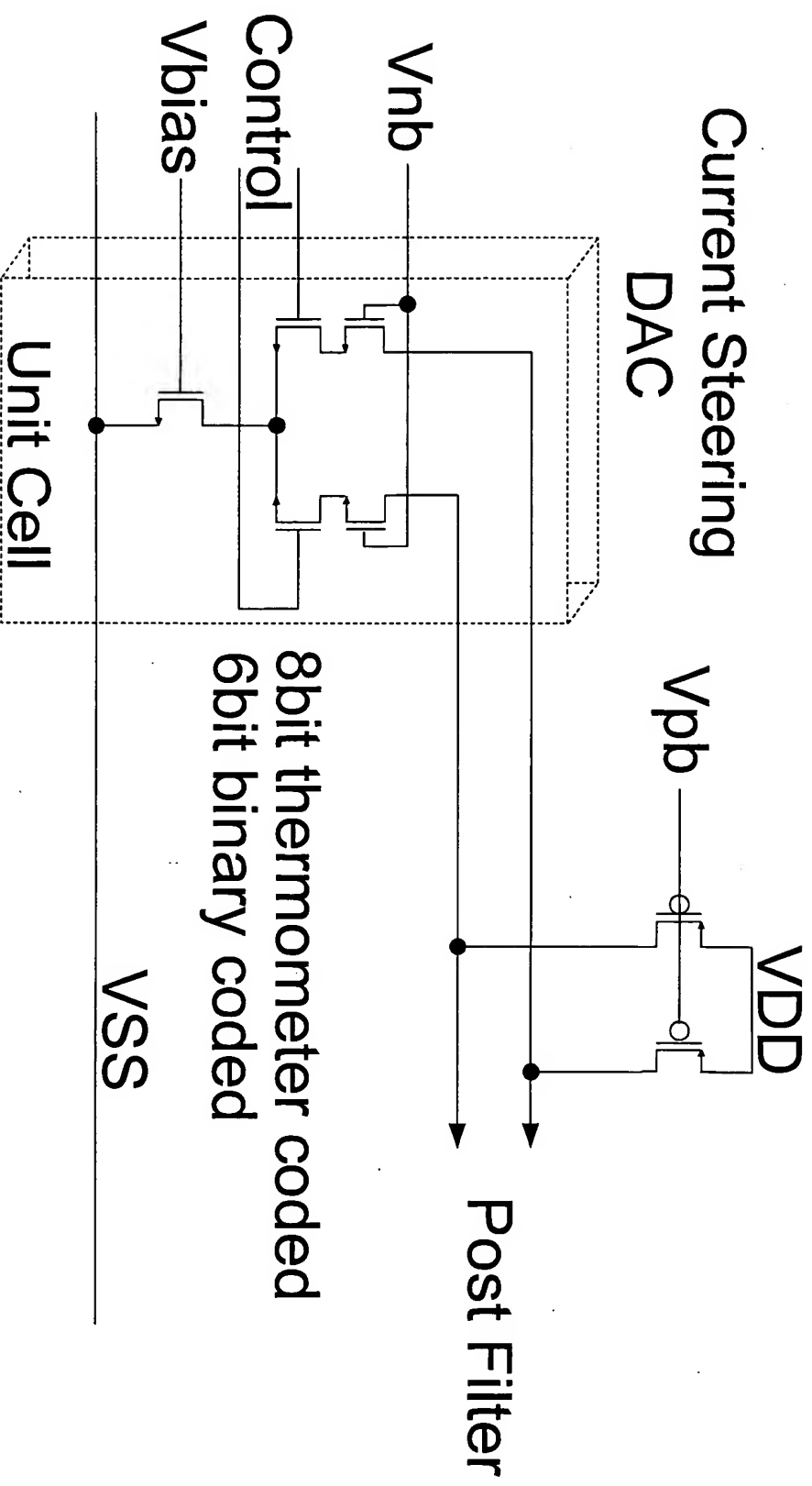
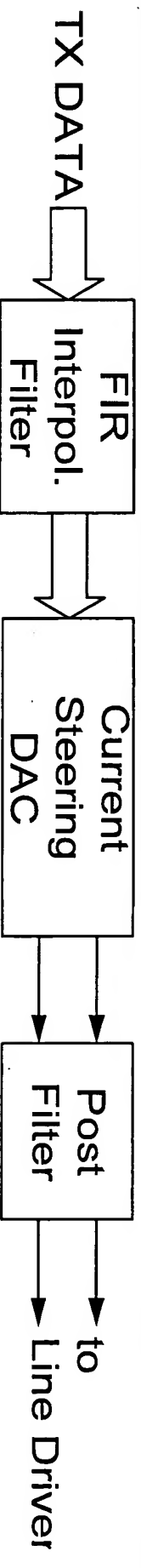
Overview continued



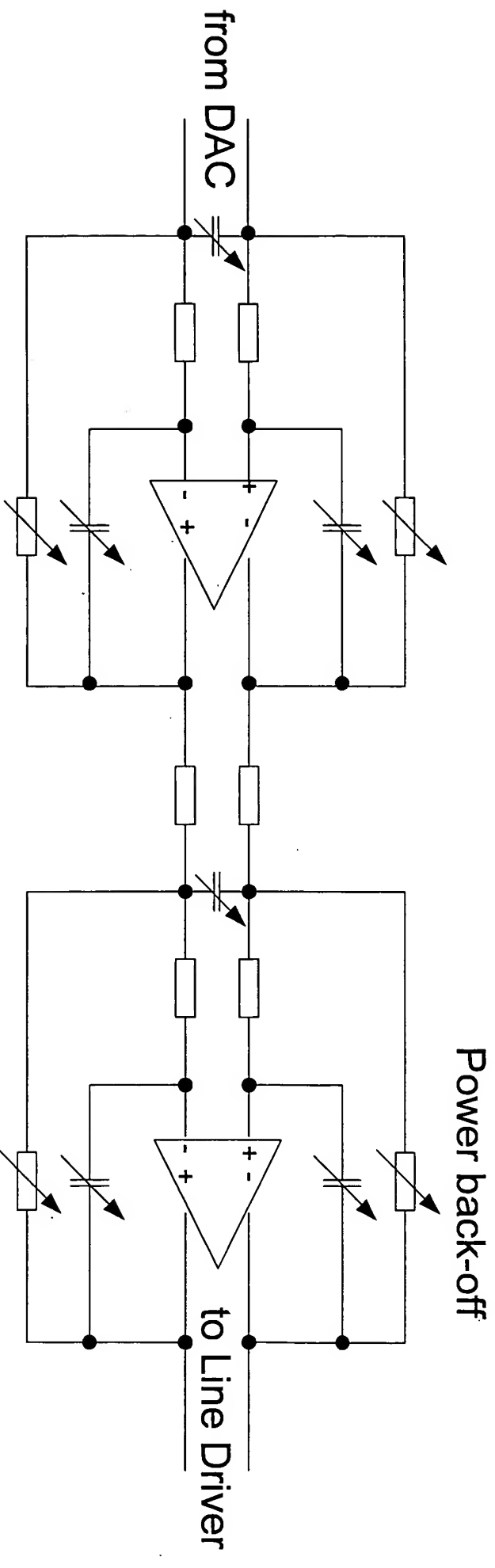
Architecture Per Channel



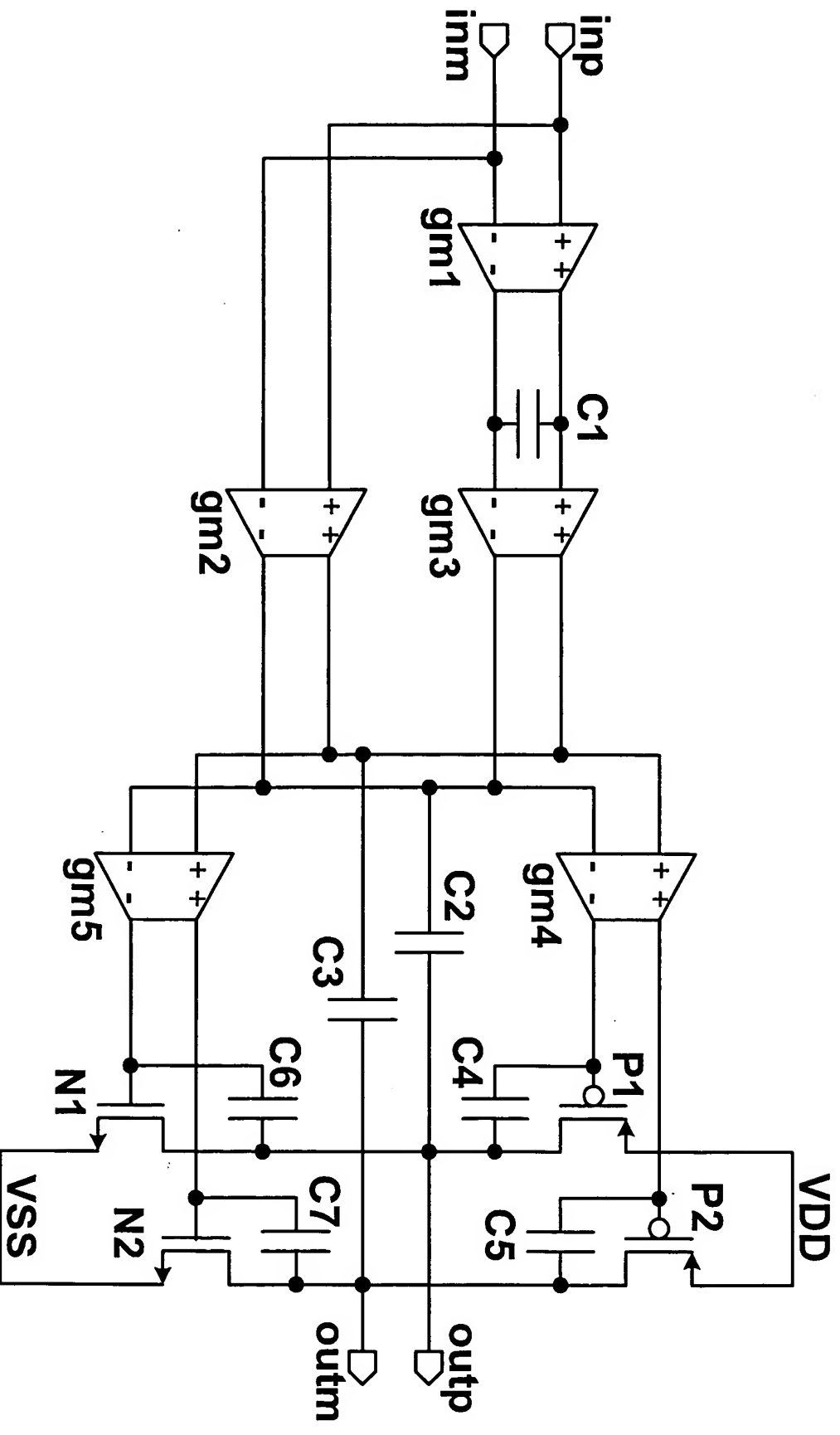
Transmitter Implementation: DAC



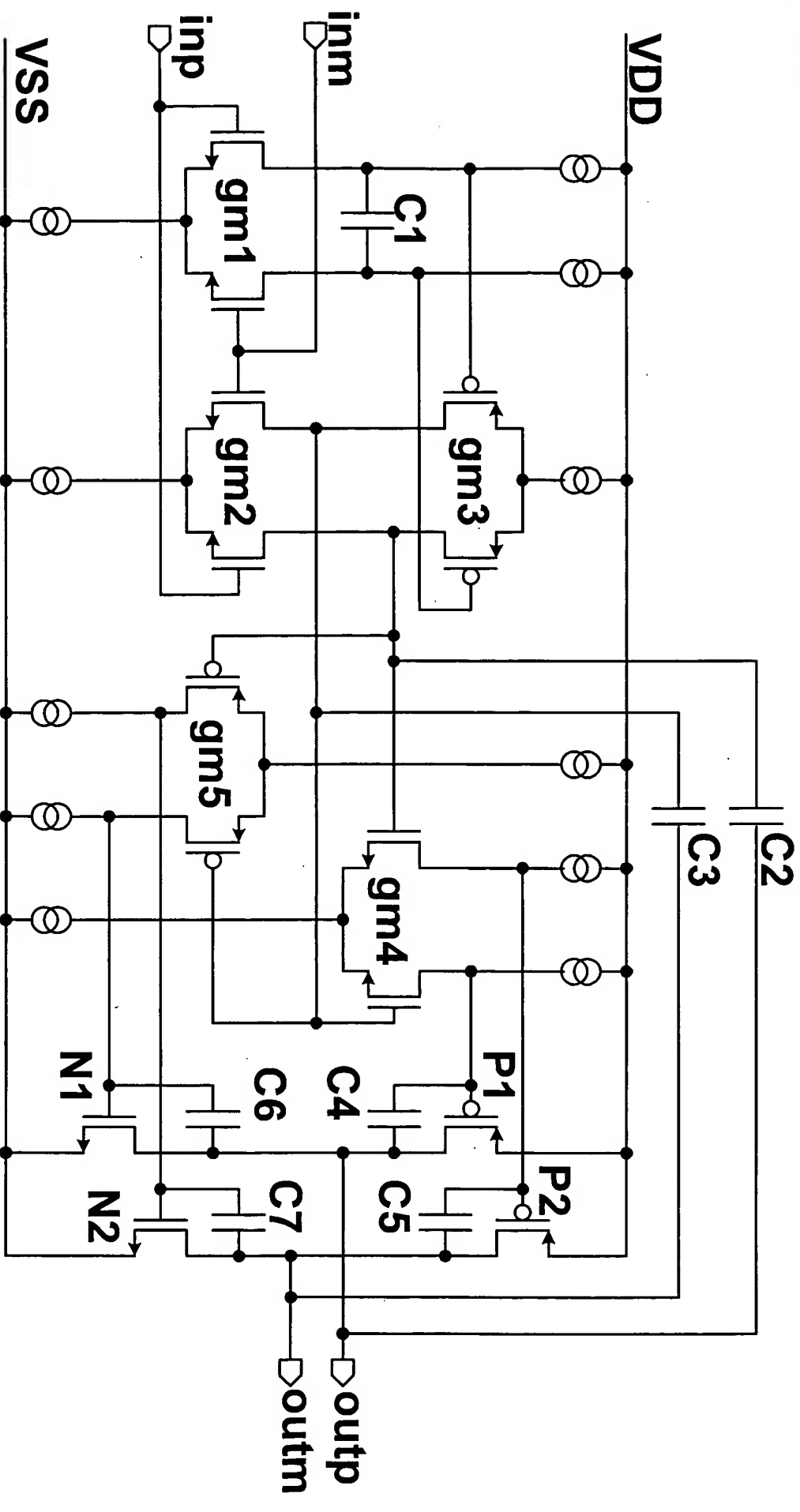
Transmitter: Post Filter



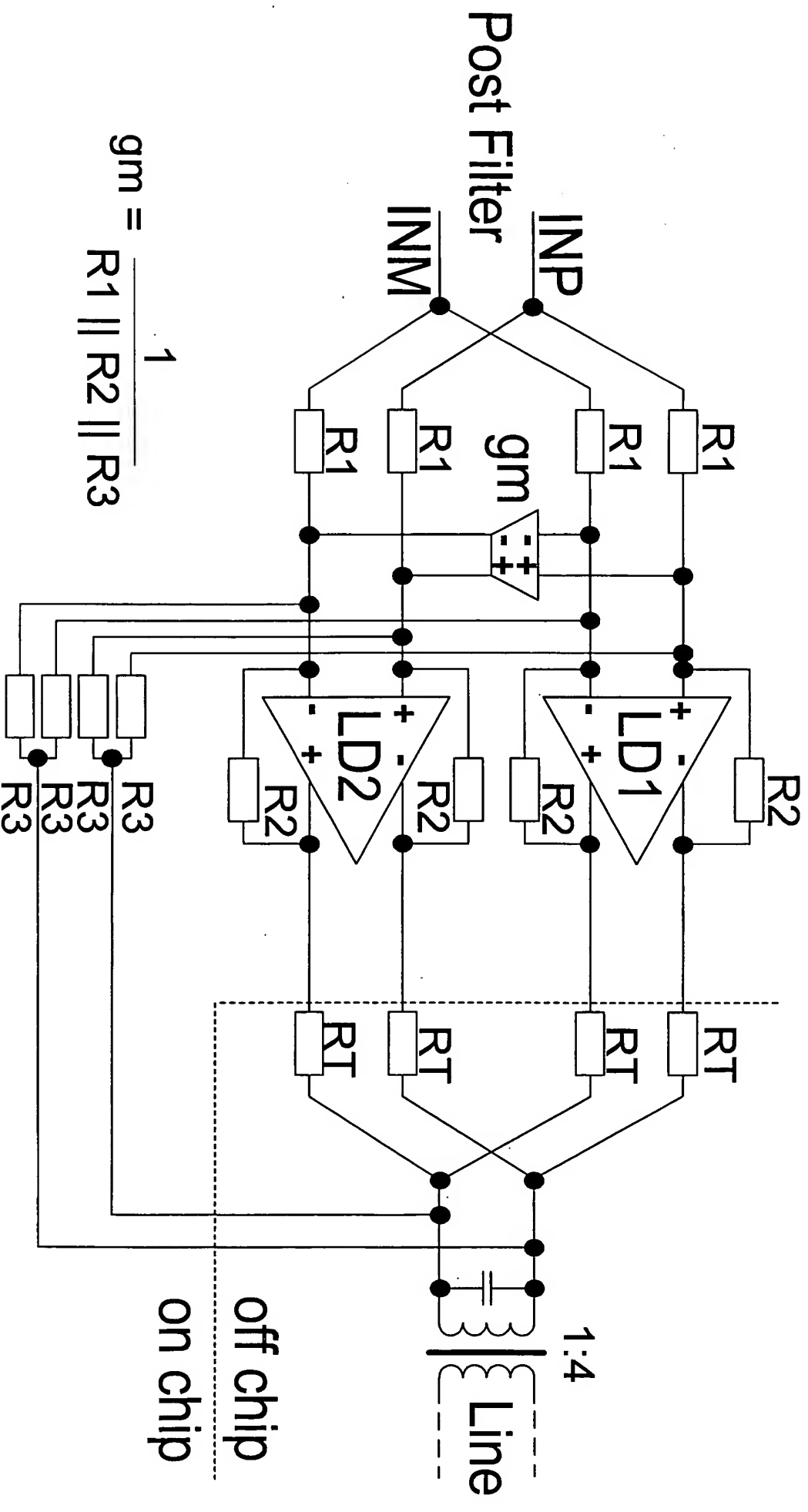
- 4th order Butterworth, f_{-3dB} 18MHz, calibrated at power up
- 14dB Power back-off in 1dB steps



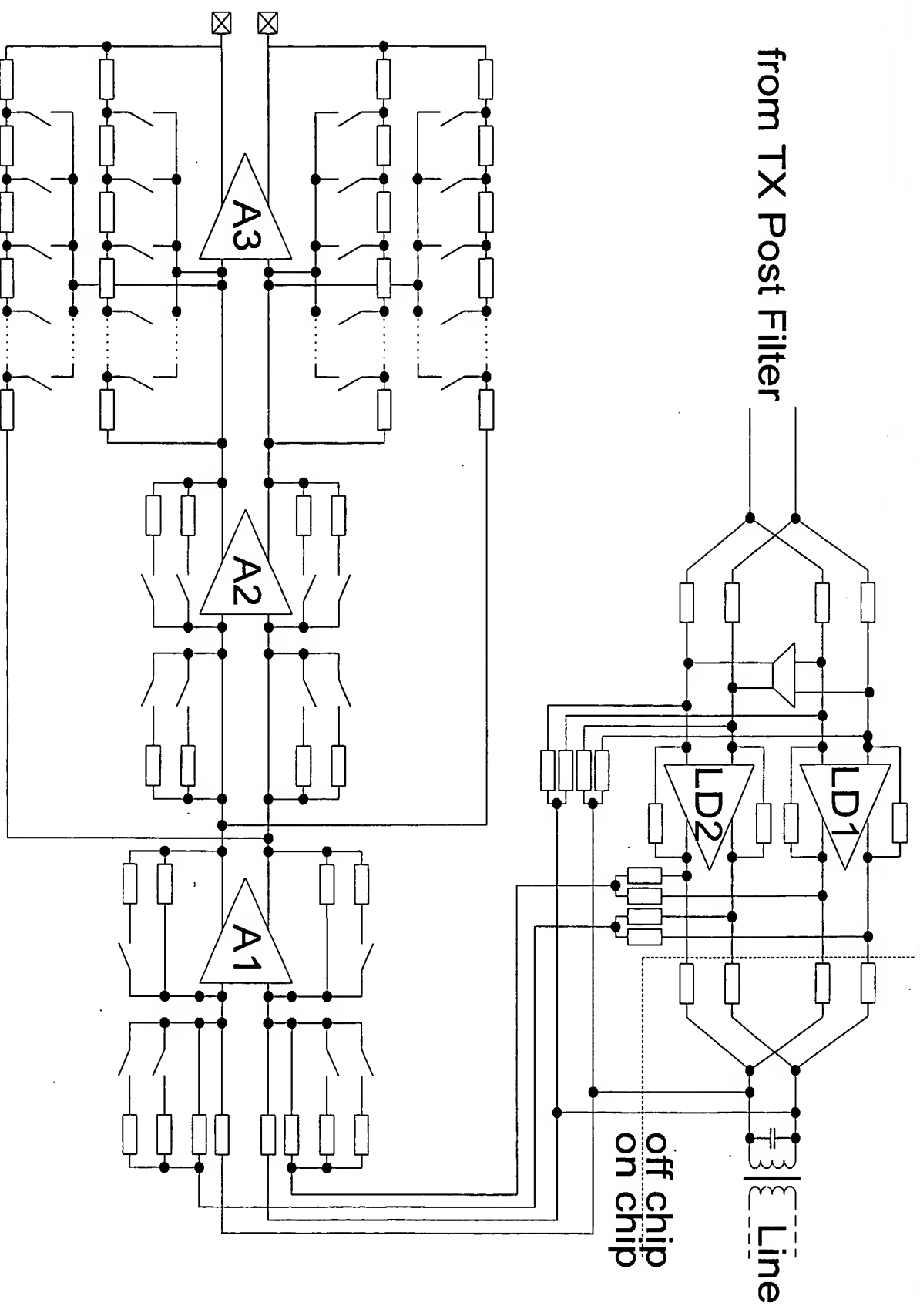
OPAMP CORE



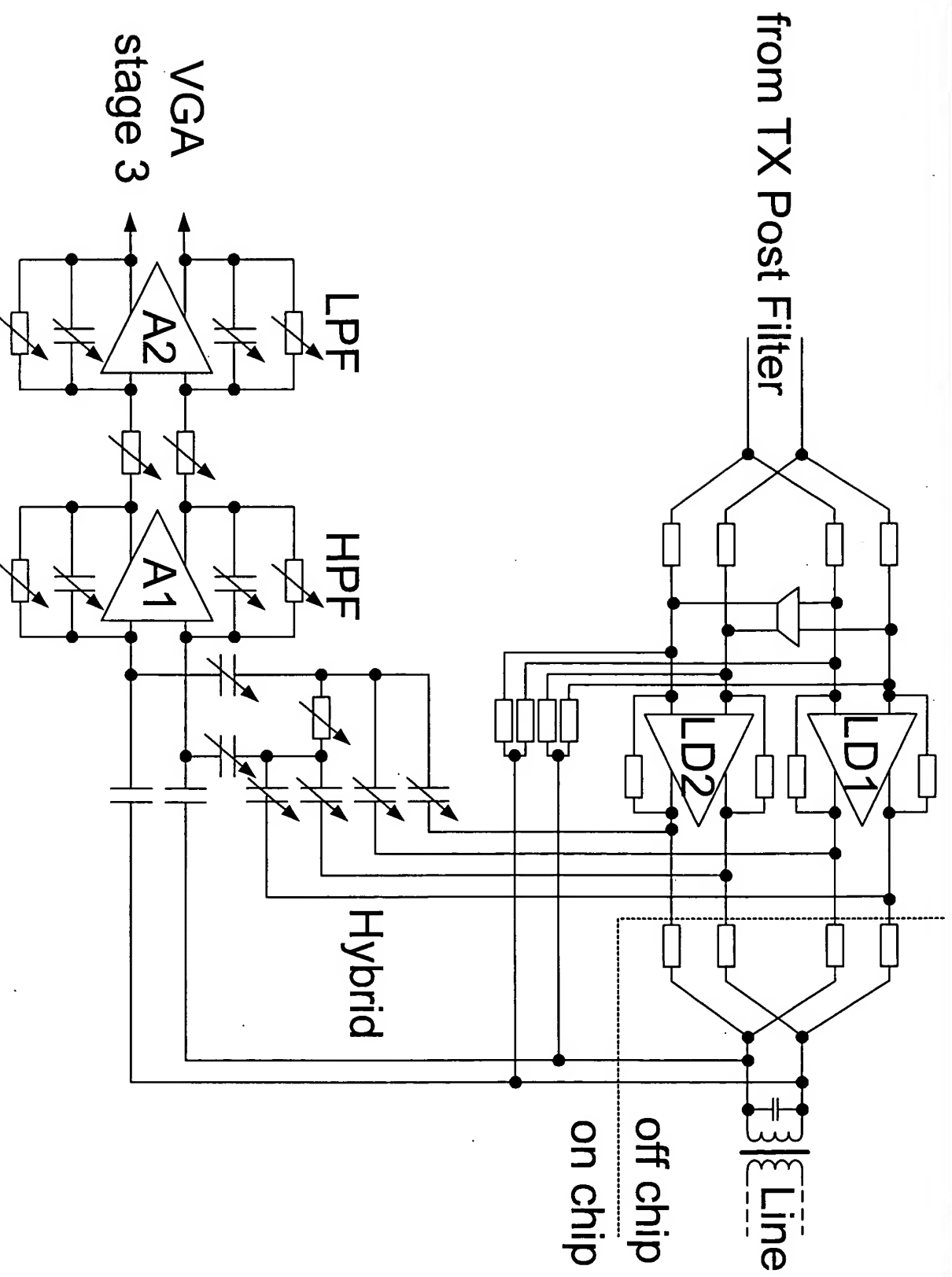
Line Driver



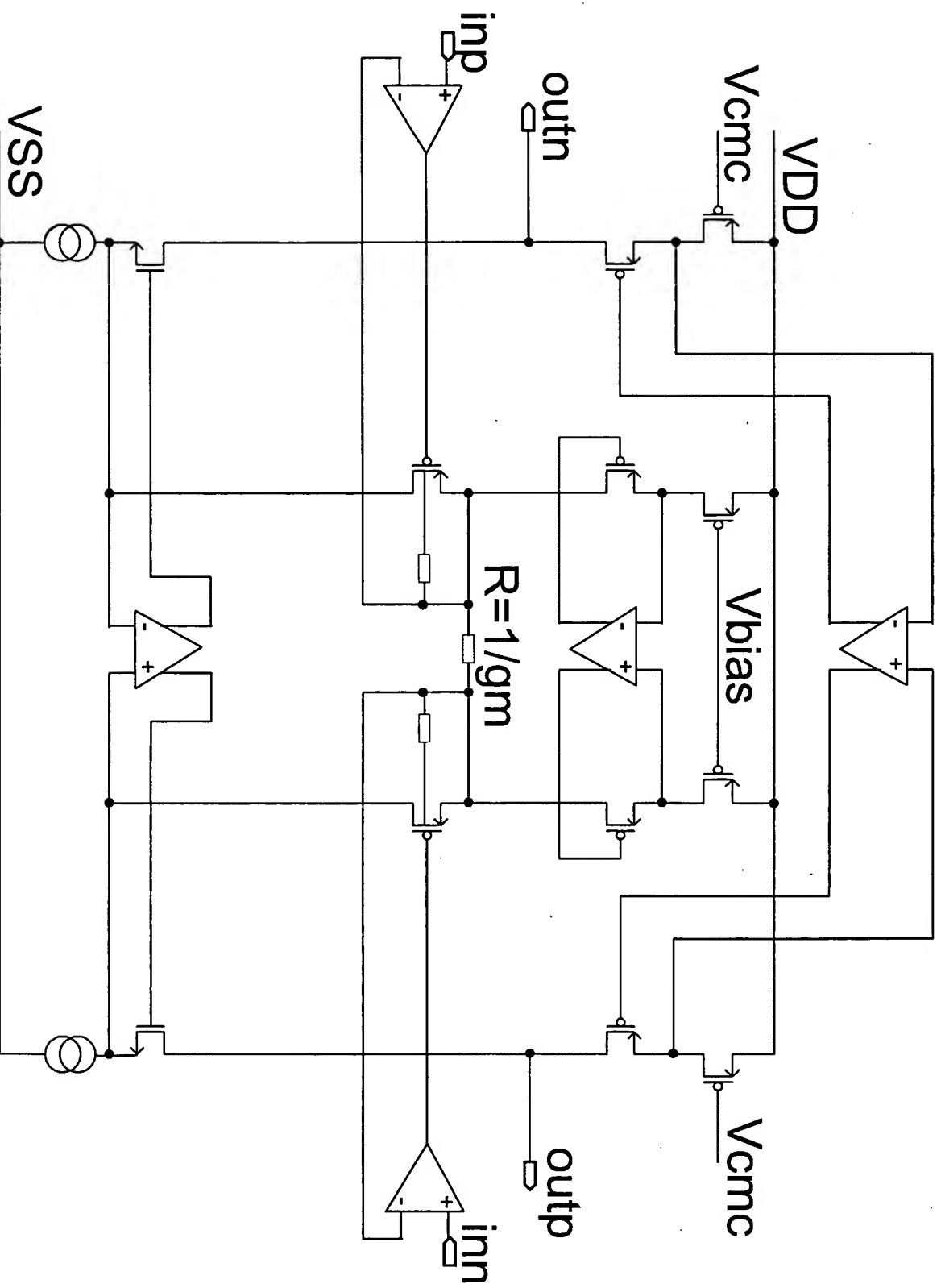
Hybrid / VGA



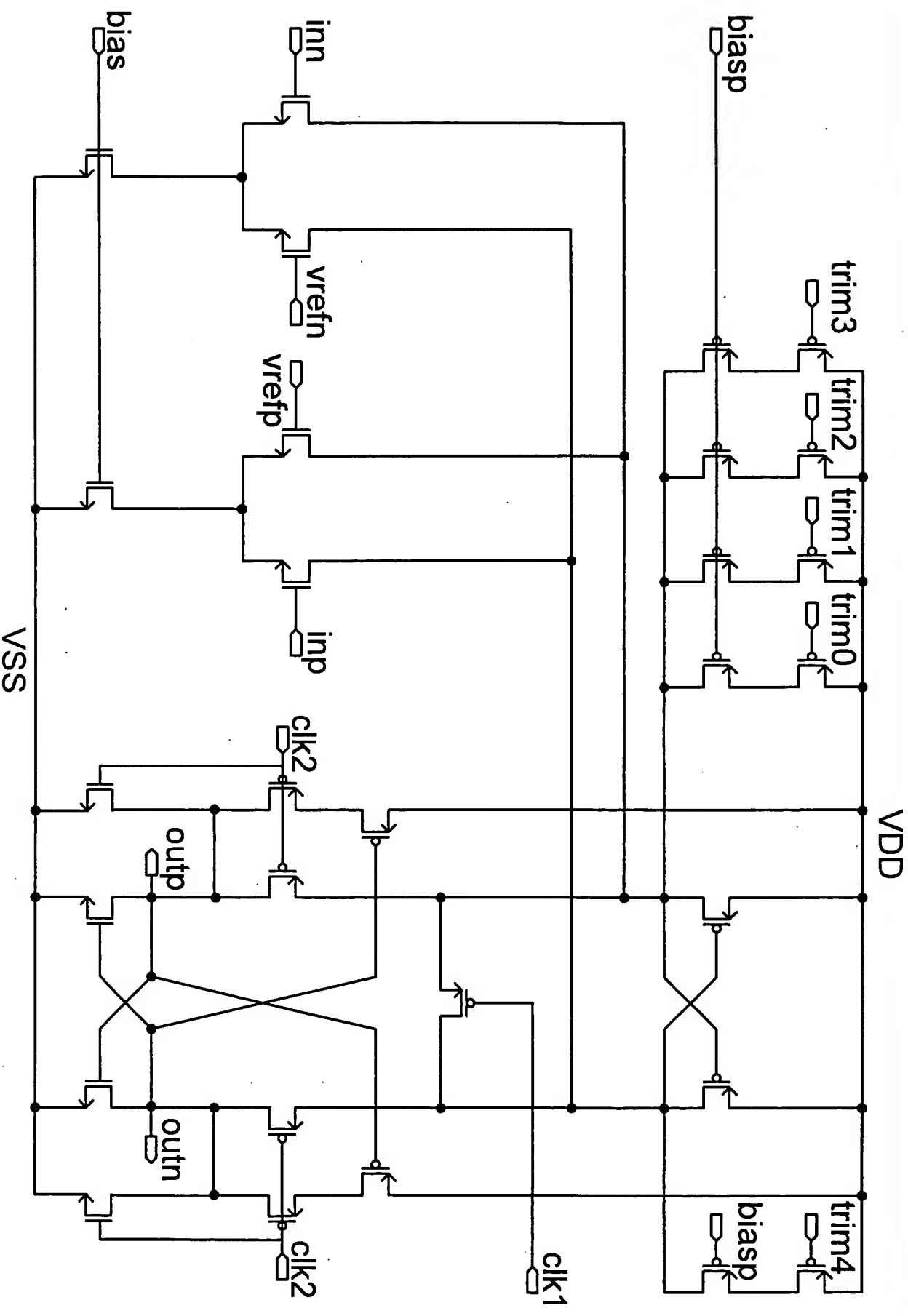
Hybrid / VGA (next revision)



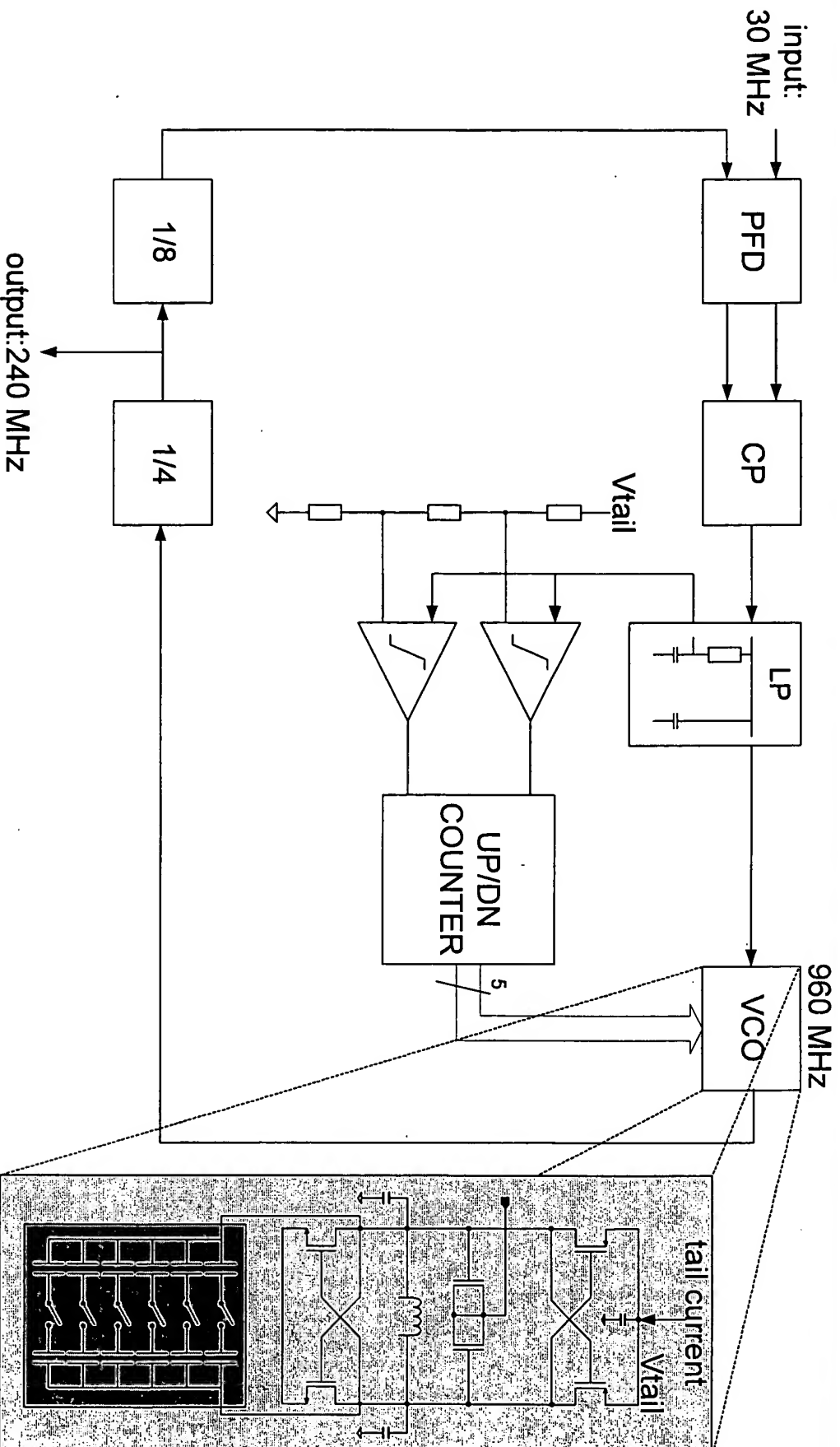
ADC GM-STAGE



ADC COMPARATOR



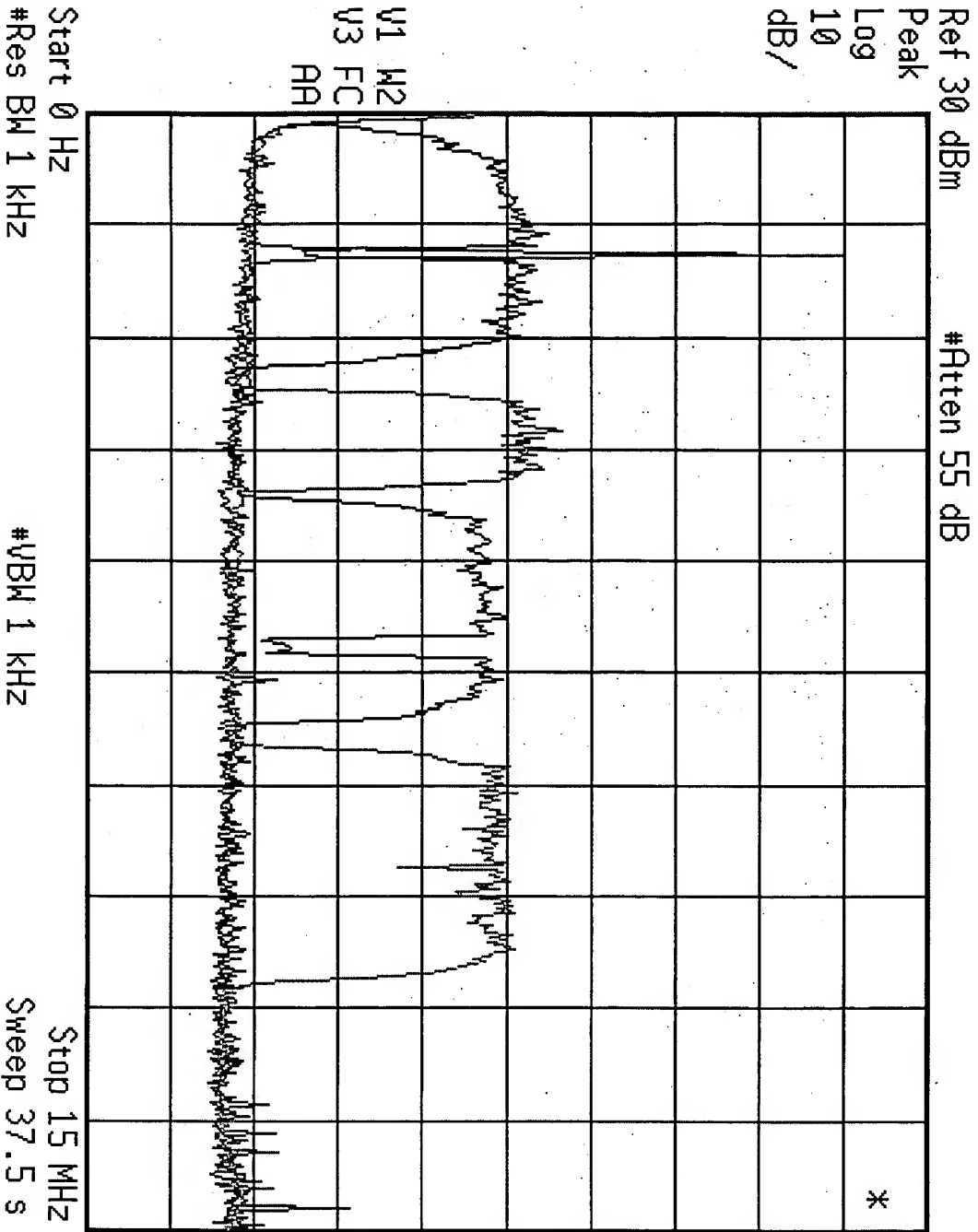
LC-PLL CIRCUIT



Measurements

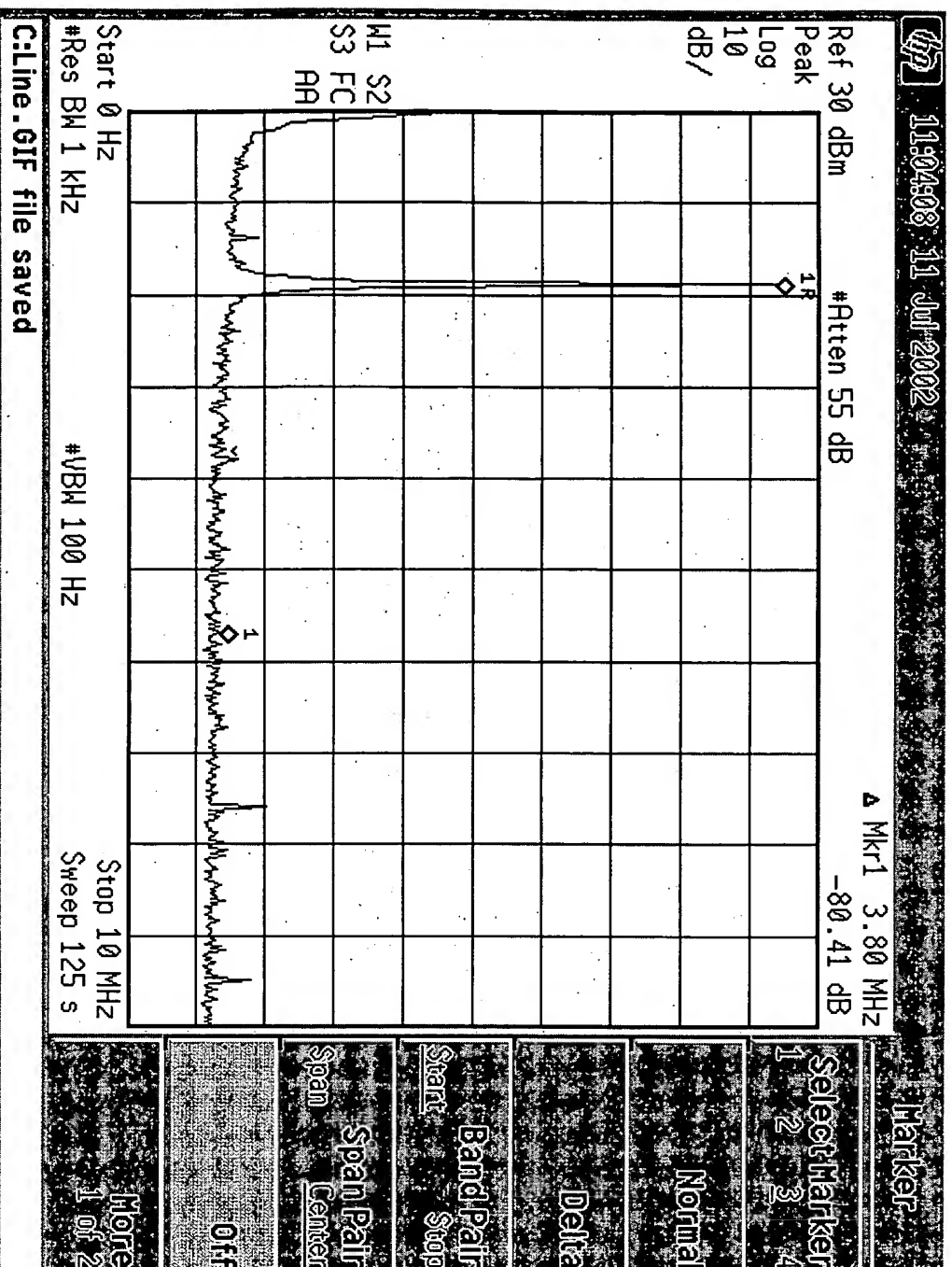
- Transmit Path and Line Driver
- Receive Path
- PLL

Transmit Path- Measurement 1



14.5 dBm signals for
power measurements
and functional tests

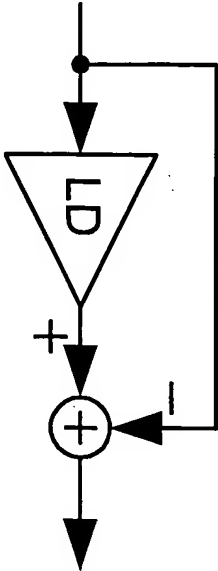
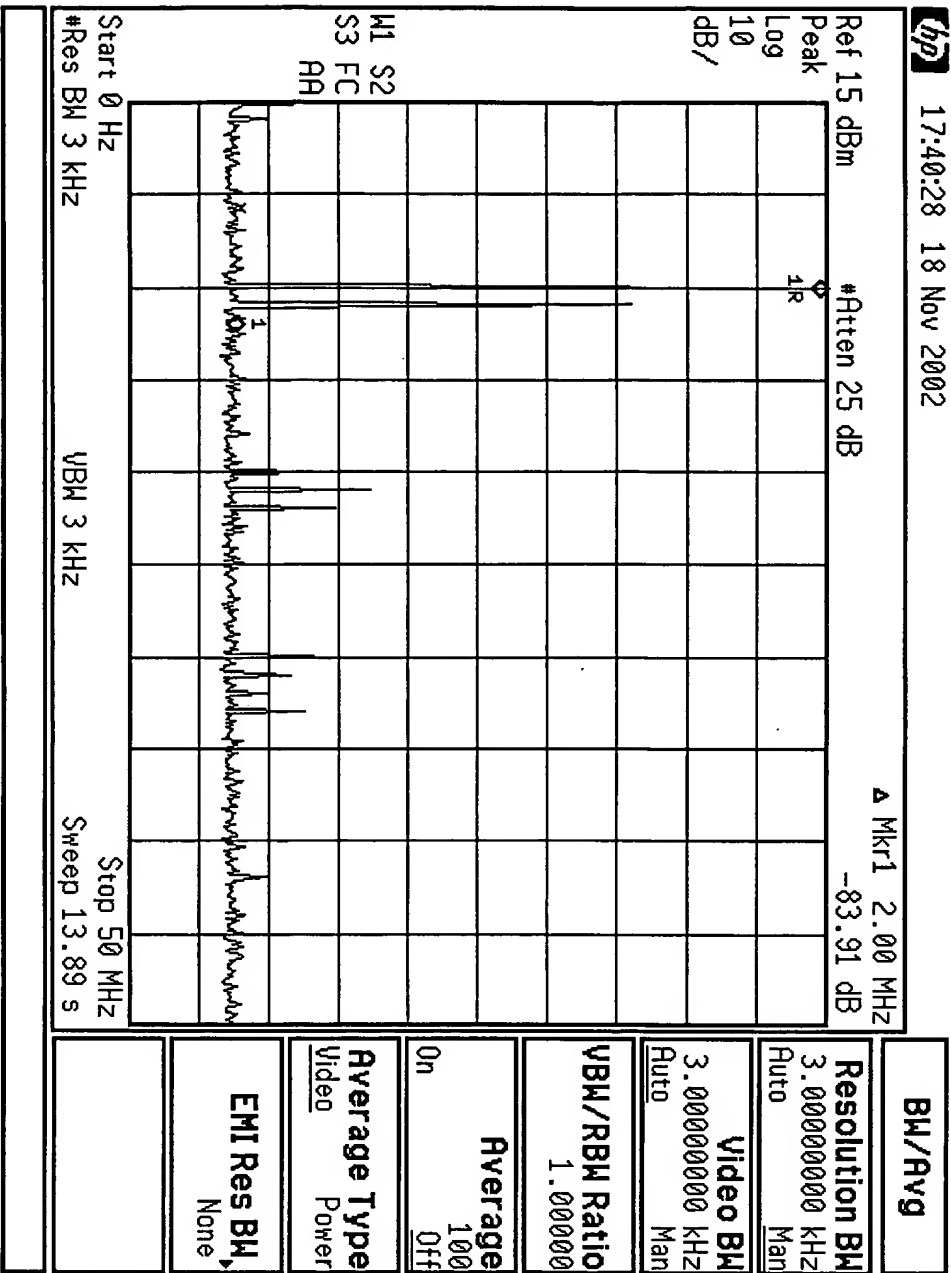
Transmit Path- Measurement 2



THD in 12MHz:

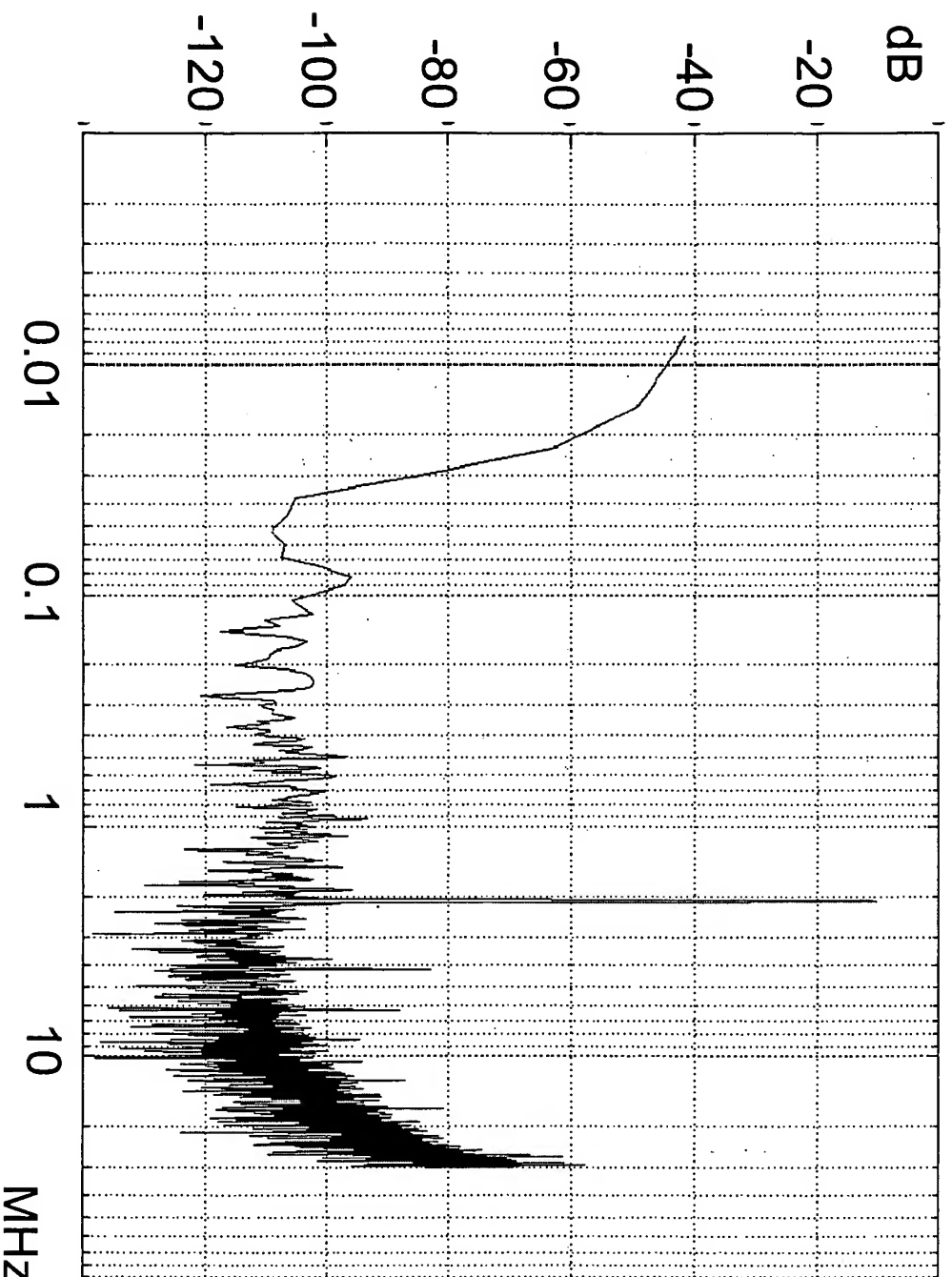
- 72.dBc @1.9MHz(0dBfs)
- 74 dBc @1.9MHz(- 3dBfs)

Line Driver IM3-Measurement



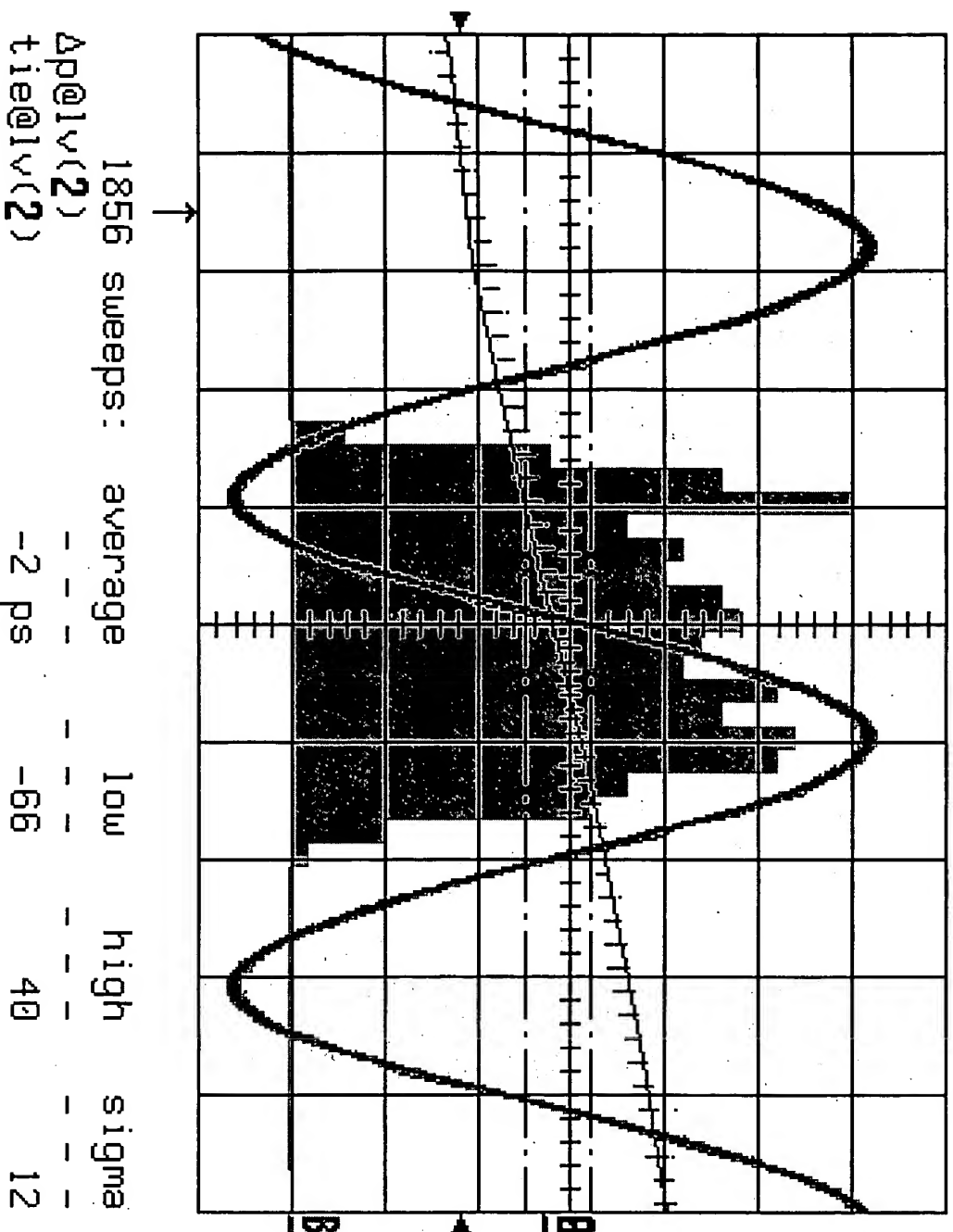
10MHz + 11MHz full scale
Input signal subtracted
IM3: below -83dBc

Receive Path- Measurement



2.1MHz (-1dBfs)
14 dB VGA gain
BW = 12MHz
SNR = 72dB
THD = 71dB

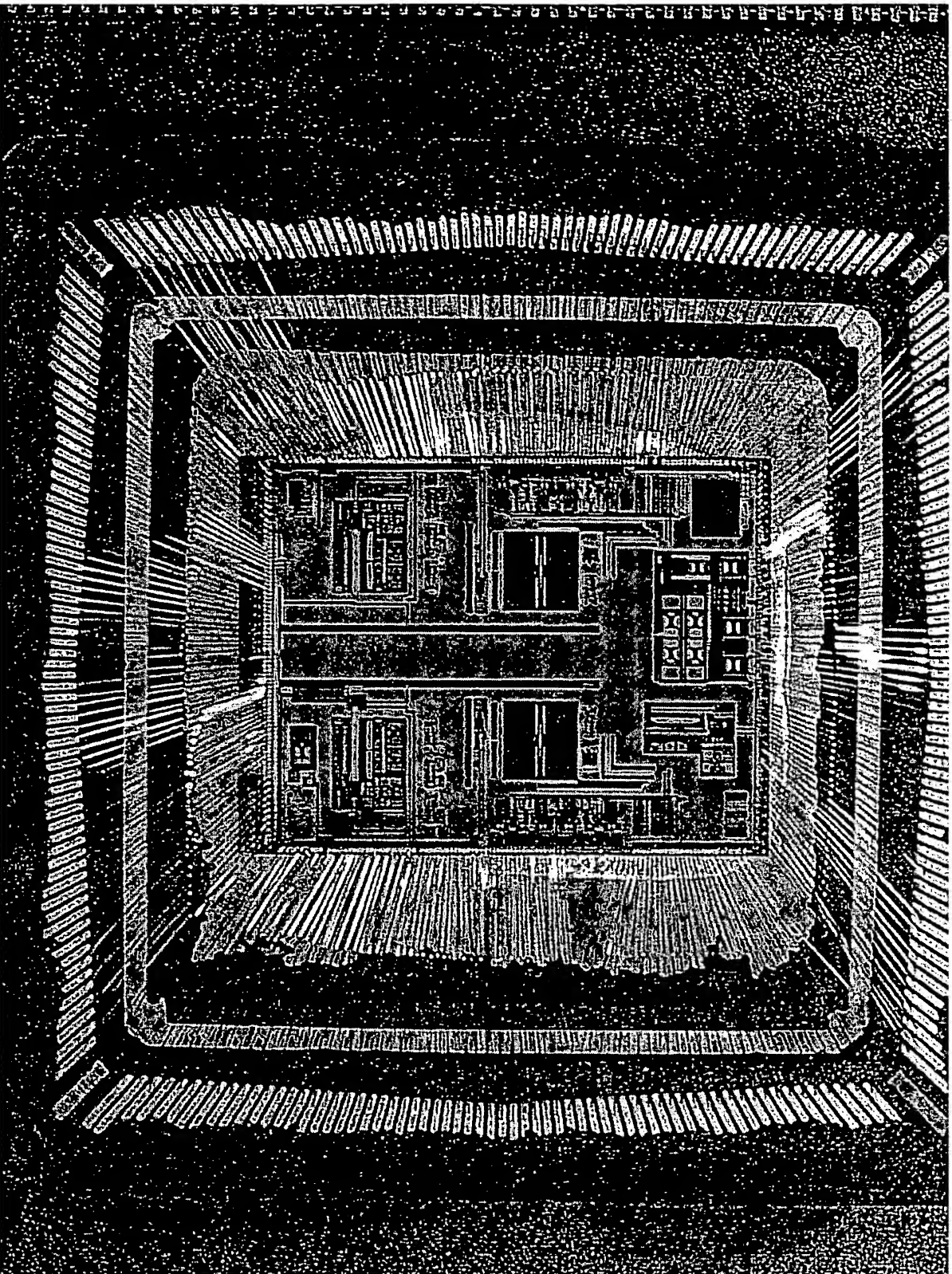
240MHz-PLL Measurement



30MHz input
240MHz output

Jitter:
12ps(rms)

Die Photo



Summary

- Dual Channel VDSL AFE
- Integrated Line Driver
- 900mW/channel power consumption at 14.5dBm line power
- 23mm²/channel (31mm² with test structures)
- 12b TX-performance at 12MHz signal bandwidth
- 12b RX-performance at 12MHz signal bandwidth

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